PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Bijan Davari, et al.

Examiner: Long Pham

Serial No.: 09/975,435

Art Unit: 2814

Filed: October 11, 2001

Docket: YOR919990101US2 (16322)

For: PATTERNED SOI REGIONS ON SEMICONDUCTOR CHIPS

Dated: May 19, 2003

Commissioner for Patents
Alexandria, VA 22313

SUBMISSION OF DECLARATION UNDER 37 CFR §1.131

Sir:

In connection with the Amendment and Response dated April 14, 2003, applicants submit herewith an executed copy of the §1.131 Declaration: two copies of the Declaration are enclosed--one copy includes Mr. Davari's, Mr. Sadana's and Mr. Shahidi's signatures, the other includes Mr. Tiwari's signature. The 131 Declaration was used in the aforementioned Amendment and Response to antedate U.S. Patent No. 6,063,652 to Kim, which reference was cited in the Office Action dated November 13, 2002.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents Alexandria, VA 22313 on May 19, 2003.

Dated: May 19, 2003

Mishelle Mustafa

Applicants respectfully submit that the 131 Declaration clearly indicates that the claimed invention was completed in the laboratories of IBM Corporation in Yorktown Heights, NY prior to the effective filing date of Kim, i.e., February 25, 1999.

As such, applicants have antedated the Kim disclosure. The 103 rejection, which included the Kim disclosure, is thus based on solely the disclosures of Japanese Patent No. 09064323 A and U.S. Patent No. 5,494,846 to Yamazaki. As argued in applicants' Amendment and Response, the combination of JP '323 and Yamazaki does not render the claimed invention obvious.

Wherefore, reconsideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,

Leslie S. Szivos
Registration No. 39,394

LSS/sf
Enclosures Declaration under 1.131
Exhibits A and B

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Commissioner for Patents
Washington, DC 20231

DECLARATION UNDER 37 C.F.R. §1.131

Sir:

We, Bijan Davari, Devendra K. Sadana, Ghavam G. Shahidi and Sandip Tiwari, hereby declare that:

1. We are the applicants named in U.S. Patent Application Serial No. 09/975,435, filed October 11, 2001.

2. We made the invention which is disclosed and claimed in the present application, in the United States, prior to February 25, 1999, which is the effective U.S. filing date of U.S. Patent No. 6,063,652 to Kim ("Kim").

3. As evidence of completion of said invention prior to the effective filing date of Kim annexed hereto are Exhibits A and B. Exhibits A and B consist of true photocopies of a write-up prepared by us (with hand made sketches and TEM's) as well as an IBM invention disclosure (with hand made sketches) which evidence that the claimed invention was developed in the laboratories at IBM Corporation in Yorktown Heights, NY prior to the February 25, 1999 effective filing date of Kim. The activity contributing to the development of the claimed invention was conducted by us or by other

scientists and/or technicians working under our direct supervision and control prior to the effective filing date of Kim. Dates and names have been redacted in the preparation of the photocopies contained in the attached exhibits.

4. The instant application is directed to semiconductor structures including a semiconductor substrate containing silicon having an upper surface, said substrate having at least one silicon-on-insulator (SOI) region and at least one bulk semiconductor region adjacent to the SOI region. The instant application is also directed to methods of forming the semiconductor structures of the present application. We have been advised by counsel that method Claims 35-56 are the subject matter of the instant application currently being prosecuted in the above-identified application. In broad terms, the method of the present invention comprises the steps of forming a first mask having an opening therein on a Si-containing substrate; implanting oxygen ions through the opening in the first mask into the substrate; and annealing the substrate to form a plurality of first buried oxide regions below a Si-containing layer whereby spaced apart SOI regions are formed.

In some embodiments of the present invention, the Si-containing substrate includes trenches formed therein. It that embodiment of the claimed invention, the method includes the steps of selecting a substrate containing Si having a plurality of trenches therein; forming a first mask on the substrate having an opening to expose a trench portion, and implanting oxygen through the openings into the substrate and trench portion. The implanting step employed in this embodiment includes a step of plasma immersion ion implantation of oxygen whereby the oxygen ions pass through the

sidewalls of the trench portion to form a buried oxide layer with respect to the sidewalls of the trench.

5. Exhibit A is a written disclosure that was prepared by us and submitted to counsel prior to the effective filing date of Kim. The written disclosure provides a detailed description of the present invention as well as providing further drawings that illustrate the structures and methods of the present application. In the written disclosure, it is mentioned that patterned SOI regions of the invention are formed by implanting oxygen through a dielectric mask and then annealing. Five kinds of structures containing patterned SOI regions are mentioned and shown in the hand drawn sketches.The written disclosure also includes TEMs which demonstrate that we have actually made structures using the claimed method prior to the effective filing date of Kim, i.e., prior to February 25, 1999.

6. Exhibit B is a photocopy of the invention disclosure entitled "Patterned SOI by Oxygen Implantation" along with three sheets of hand drawn sketches that were submitted by us prior to the effective filing date of Kim. The invention disclosure discusses, under the key idea of invention section, an SOI wafer and integrated circuit chip having SOI islands surrounded by bulk silicon that is formed using a mask and ion implantation. The key idea section also discusses an SOI wafer and an integrated circuit chip with a trench having horizontal and vertical buried oxide regions with respect to the wafer surface and the trench sidewalls. The hand drawn sketches show how the various structures mentioned in the key idea invention section of the original disclosure are made.

The first drawing on the first sheet shows the formation of a buried oxide region into a Si-containing substrate using a first mask and ion implantation which is

represented by the arrows. The second drawing on the first sheet shows the formation of a structure having a top Si-containing layer of variable thickness using a mask which is thin enough to allow oxygen ions to be implanted into the substrate. Note that the buried oxide region created using this method is closer to the upper surface of the substrate in the region including the first mask as compared to the buried oxide region formed in regions not containing the mask. The third hand drawn sketch shows a structure that is formed having a buried oxide region in contact with the upper surface of the substrate and other buried oxide region which is not in contact with the upper surface of the substrate. A mask and ion implantation are used in making this structure as well.

The second sheet of drawings, which includes a single figure, shows a resultant structure that can be formed using the SOI substrates provided by the claimed method.

The third sheet of drawings shows a structure including a Si-containing substrate having a trench region formed therein having horizontal and vertical buried oxides regions with respect to the upper surface of the substrate and the trench sidewalls, respectively. Note that this sketch shows ions being implanted through the upper surface of the substrate as well as the sidewalls of the trench.

7. We further declare that all statements made herein of our knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 5/8/03

Bijan Davari

Date: 5/1/03

Devendra K. Sadana

Date: 5/7/03

Ghavam G. Shahidi

Date: _____

Sandip Tiwari